

CLEAN VERSION OF THE ENTIRE SET OF CLAIMS

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1. (AMENDED) An apparatus comprising:
a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and
a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request corresponds to at least P of the stored prefetch addresses, P being a non-zero integer, the canceler including a gating circuit to disable the access request to the memory when the access request is canceled.

2. The apparatus of claim 1 wherein the storage circuit comprises:
a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

3. The apparatus of claim 2 wherein the queue comprises:
a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

4. The apparatus of claim 3 wherein the canceler comprises:
a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

5. The apparatus of claim 4 wherein the canceler further comprises:
a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

6. The apparatus of claim 4 wherein the matching circuit comprises:
a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

1 7. The apparatus of claim 4 wherein the matching circuit comprises:
2 a plurality of comparators to compare the current prefetch address with contents of
3 the plurality of registers, the comparators generating comparison results.

1 8. The apparatus of claim 7 wherein the cancel generator comprises:
2 a comparator combiner coupled to the comparators to combine the comparison
3 results, the combined comparison results corresponding to the cancellation request.

1 9. The apparatus of claim 2 wherein the canceler comprises:
2 a matching circuit having an argument register to store the current prefetch address
3 for matching with entries of the CAM.

1 10. The apparatus of claim 9 wherein the canceler further comprises:
2 a cancellation generator to generate a match indicator when the current prefetch
3 address matches at least P of the entries, the match indicator corresponding to the
4 cancellation request.

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1 11. (AMENDED) A method comprising:
2 storing a plurality of prefetch addresses in a storage circuit, the plurality of prefetch
3 addresses corresponding to most recent access requests from a processor, the prefetcher
4 generating an access request to a memory when requested by the processor; and
5 canceling the access request when the access request corresponds to at least P of the
6 stored prefetch addresses, P being a non-zero integer; and
7 disabling the access request to the memory by a gating circuit when the access request
8 is canceled.

1 12. The method of claim 11 wherein storing comprises:
2 storing the plurality of prefetch addresses in one of a queue with a predetermined size
3 and a content addressable memory (CAM).

1 13. The method of claim 12 wherein storing the plurality of prefetch addresses in
2 the queue comprises:

3 storing the plurality of prefetch addresses in a plurality of registers cascaded to shift
4 the prefetch addresses each time the processor generates a prefetch request.

1 14. The method of claim 13 wherein canceling comprises:
2 matching a current prefetch address associated with the access request with the stored
3 prefetch addresses.

1 15. The method of claim 14 wherein canceling further comprises:
2 generating a cancellation request to the prefetcher when the current prefetch address
3 matches to the at least P of the stored prefetch addresses.

1 16. The method of claim 14 wherein matching comprises:
2 comparing the current prefetch address with each of the stored prefetch addresses.

1 17. The method of claim 14 wherein matching comprises:
2 comparing the current prefetch address with contents of the plurality of registers, the
3 comparators generating comparison results.

1 18. The method of claim 17 wherein generating the cancellation request
2 comprises:
3 combining the comparison results, the combined comparison results corresponding to
4 the cancellation request.

1 19. The method of claim 12 wherein canceling comprises:
2 storing the current prefetch address in an argument register for matching with entries
3 of the CAM.

1 20. The method of claim 9 wherein canceling further comprises:
2 generating a match indicator when the current prefetch address matches at least P of
3 the entries, the match indicator corresponding to the cancellation request.

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21 (AMENDED) A system comprising:
a processor to generate prefetch requests;

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3 a memory to store data; and
4 a chipset coupled to the processor and the memory, the chipset comprising:
5 a prefetcher to generate an access request to the memory when requested by
6 the processor;
7 a prefetch monitor circuit coupled to the prefetcher, the prefetch monitor
8 circuit comprising:
9 a storage circuit coupled to the prefetcher to store a plurality of
10 prefetch addresses, the plurality of prefetch addresses corresponding to most
11 recent access requests from the processor; and
12 a canceler coupled to the storage circuit and the prefetcher to cancel
13 the access request when the access request corresponds to at least P of the
14 stored prefetch addresses, P being a non-zero integer, the canceler including a
15 gating circuit to disable the access request to the memory when the access
16 request is canceled.

1 22. The system of claim 21 wherein the storage circuit comprises:
2 a storage element to store the plurality of prefetch addresses from the most recent
3 access requests by the processor, the storage element being one of a queue with a
4 predetermined size and a content addressable memory (CAM).

1 23. The system of claim 22 wherein the queue comprises:
2 a plurality of registers cascaded to shift the prefetch addresses each time the processor
3 generates an access request.

1 24. The system of claim 23 wherein the canceler comprises:
2 a matching circuit to match a current prefetch address associated with the access
3 request with the stored prefetch addresses.

1 25. The system of claim 24 wherein the canceler further comprises:
2 a cancel generator coupled to the matching circuit to generate a cancellation request
3 to the prefetcher when the current prefetch address matches to the at least P of the stored
4 prefetch addresses.

1 26. The system of claim 24 wherein the matching circuit comprises:
2 a plurality of comparators to compare the current prefetch address with each of the
3 stored prefetch addresses.

1 27. The system of claim 24 wherein the matching circuit comprises:
2 a plurality of comparators to compare the current prefetch address with contents of
3 the plurality of registers, the comparators generating comparison results.

1 28. The system of claim 27 wherein the cancel generator comprises:
2 a comparator combiner coupled to the comparators to combine the comparison
3 results, the combined comparison results corresponding to the cancellation request.

1 29. The system of claim 22 wherein the canceler comprises:
2 a matching circuit having an argument register to store the current prefetch address
3 for matching with entries of the CAM.

1 30. The system of claim 29 wherein the canceler further comprises:
2 a cancellation generator to generate a match indicator when the current prefetch
3 address matches at least P of the entries, the match indicator corresponding to the
4 cancellation request.